

Amendments of the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A programmable logic resource comprising:

an input/output (I/O) buffer that receives data from circuitry external to the programmable logic resource and generates a plurality of outputs;

a crossbar switch that receives the plurality of outputs from the I/O buffer and generates a plurality of outputs, wherein the crossbar switch is configured to send at least one of the plurality of outputs from the I/O buffer to a corresponding one of the plurality of outputs of the crossbar switch; and

an intellectual property block that receives the plurality of outputs of the crossbar switch for processing;

wherein the programmable logic resource is embedded in a package having a plurality of pins through which the external circuitry sends data, the programmable logic resource having a plurality of I/O ports located along the periphery of the programmable logic resource, wherein at least one of the plurality of pins sends data to a nearest available one of the plurality of I/O ports such that the at least one pin corresponds to other than the nearest available I/O port.

2. (Currently Amended) The programmable logic resource of claim 1 wherein the I/O buffer:

receives the data at the plurality of I/O ports located along the periphery of the programmable logic resource; and

decodes the data to generate the plurality of outputs.

3-4. (Cancelled)

5. (Original) A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

a programmable logic resource as defined in claim 1 coupled to the processing circuitry and the memory.

6. (Original) A printed circuit board on which is mounted a programmable logic resource as defined in claim 5.

7. (Original) The printed circuit board defined in claim 6 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic resource.

8. (Original) The printed circuit board defined in claim 6 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic resource.

9. (Currently Amended) A printed circuit board comprising:

processing circuitry mounted on the printed circuit board;

a memory mounted on the printed circuit board and coupled to the processing circuitry; and

a package having a plurality of pins mounted on the printed circuit board at fixed pin locations and coupled to the processing circuitry and the memory at the fixed pin locations, the package having embedded therein a programmable logic resource having a plurality of input/output (I/O) ports located along the periphery of the programmable logic resource ~~[[and]]~~, wherein at least one of the plurality of pins is coupled to a nearest available one of the plurality of pins I/O ports such that the at least one pin corresponds to other than the nearest available I/O port, and wherein the programmable logic resource comprises circuitry configured to send data from ~~at least one of the plurality of nearest available~~ I/O ports to a corresponding one of a plurality of data ports in an intellectual property block for processing.

10. (Cancelled)

11. (Original) The printed circuit board of claim 9 wherein the programmable logic resource further comprises an I/O buffer that receives the data from the plurality of I/O ports and decodes the data for output to the circuitry.

12. (Original) The printed circuit board of claim 9 wherein the circuitry is a configurable crossbar switch.

13. (Original) The printed circuit board of claim 9 wherein the circuitry is a dynamically adjustable crossbar switch.

14. (Currently Amended) A method of improving connectivity between signaling input/output (I/O) and an intellectual property block in a programmable logic resource comprising:

driving a signal to a fixed pin location on a circuit board upon which a package, having embedded therein the programmable logic resource, is mounted;

routing the signal from the fixed pin location to a nearest available I/O port located along the periphery of the programmable logic resource, wherein the fixed pin location corresponds to other than the nearest available I/O port; and

configuring a crossbar switch to route the signal from the nearest available I/O port to a corresponding data port in the intellectual property block for processing.

15. (Original) The method of claim 14 wherein driving the signal comprises sending the signal as output from one of processing circuitry and a memory.

16. (Original) The method of claim 14 wherein the signal is a low voltage differential signal.

17. (Original) The method of claim 14 further comprising decoding the signal received from the nearest available I/O port for output to the crossbar switch.

18. (Original) The method of claim 14 further comprising configuring the crossbar switch during initial configuration of the programmable logic resource.

19. (Original) The method of claim 14 further comprising configuring the crossbar switch during reconfiguration of all or part of the programmable logic resource.

20. (Original) The method of claim 14 further comprising dynamically adjusting the crossbar switch while data is processing in the programmable logic resource.